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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,836	02/02/2001	Richard Bisinella	CALLINAN 207-KFM	1154

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	7

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,836	BISINELLA, RICHARD	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 1, and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton (patent No. 6,088,783) in view of Potash (patent No. 4,760,518).

2. Morton taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Plurality of circuit elements comprising arithmetic logic units (107,110,111,112,113), memory (108) and input/output unit circuits (114,115) (e.g., see fig. 1);

b) The plurality components interconnected on a grid (crossbar switch 109) wherein each of the plurality of components can be switched under program control to be connected to a predetermined selection of one or more of the plurality of components to route data through the grid for processing by the predetermined selection of one or more of the plurality of components (e.g., see col. 21, line 41-col. 22, line 55, and col. 28, lines 44-55).

3. Morton did not expressly detail (claim 1) registers interconnected by the grid. Potash however taught registers (32,34,36,38) connected to components comprising ALUs (30) via a grid (40) (fig. 1).

4. It would have been obvious to one of ordinary skill in the DP art to combine the teaching of Morton and Potash. Morton taught passing data between processor via memory with data transmitted over a grid (e.g., see col. 21, lines 41-65). One of ordinary skill would have been motivated to incorporate the Potash teachings of

connecting the registers to the grid for access in order to improve the access to the registers for transfer of data in that the access path would have been more direct and therefore have improved access (e.g., see fig. 1 and col. 5, line 51-col. 6, line 15 of Potash).

5. As per claim 3, Morton taught a grid connector and interconnection logic (702,705,707,710) (109) (e.g., see col. 21, line 41-col. 22, line 55, and col. 28, lines 44-55).

6. As per claim 4, Morton taught instruction decode (e.g., see col. 16, lines 35-65) and Potash taught a decoder that for interpreting the instruction set of the microprocessor into timed operations of the microprocessor and a grid connector which provided logic for interconnecting a predetermined one or more of the plurality of components with one or more of other components of the plurality of components on to the grid (e.g., see col. 31, line 20-col. 32, line 62).

7. As per the further limitations of claim 5, Potash taught a second grid (44) coupled to the elements connected the first grid (40)(e.g., see fig. 1).

8. Applicant's arguments with respect to claims 1,3-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pincus (patent No. 6,282,583) taught a system for memory access in a matrix processor computer (e.g., see figs. 5a, 5b, 5c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER

May 8, 2004